IBM

System/4 Pi
and Advanced
System/4 Pi
Computers

System/4 Pi Computers

System/4 Pi Computers
Military Nomenclature
IBM Model
Physical
Volume (in^3)
Weight (lb)
Dimensions (in) (h x w x d)
Power (W)
Storage (DRO Core)
Word Capacity (typical)
Minimum/Maximum
Bits per Word
Access Time (μs)
Read or Write Cycle (μs)
Electronics
Performance
Throughput (kop/s)
Add (μs)
Multiply (μs)
Divide (μs)
Number of Instructions
Floating Point
Channel
Registers
Software
Applications
Comments

CP-926/AYA-6	AN/AYK-6	CP-985/ASQ-133	CP-952/ASN-91(V)
CP-1	CP-2	CP-3	TC-2
1465 (Computer or Coupler-8K), 1689 (Coupler-16K)	1435	1540	2670
49 (Computer),41 (Coupler-8K), 59 (Coupler-16K)	47	52	80
7.4 x 10.1 x 19.6 (Computer or Coupler-8K), 7.4 x 10.1 x 22.6 (Coupler-16K)	7.4 x 10.0 x 19.4	7.7 x 10.2 x 19.6	9.5 x 12.8 x 22.0
329 (8K)/357 (16K)	240	260	325
8K 8K/16K	8K 8K/16K[1]	8K 8K/16K[1]	16K 16K
32	32	32	16
0.9 2.5	0.9 2.5	0.9 2.5	0.9 2.5
IC	IC	IC	IC
100 5.0 14.6 45.4 59 * (25 alterable) No Three 32-bit parallel outputs (260 kHz), three 32-bit parallel inputs, one 200-kHz serial, 144 DO, 24 DI, and 24 interrupts, with 4 priority levels	150 3.8 11.5 46.3 61 No One 16-bit PCO, two 16-bit ECI, one 16-bit ECO, 24 DI, 16 DO, and 8 interrupts, with 2 priority levels	150 3.8 11.5 46.3 61 No One 16-bit PCO, one 13-bit PCO and ECI-1, one 16-bit ECI, one 16-bit ECO, 24 DI, 16 DO, and 8 external interrupts, with 2 priority levels	125 5 20 21 51 No Four 16-bit serial outputs, six 16-bit serial inputs, one 13-bit parallel PCI, two 13-bit parallel PCI, two external interrupts, 25 DO, 74 DI, three program-controlled pulse outputs, and three pulse-counter inputs
1 hard; 2 soft	1 hard; 2 soft	1 hard; 2 soft	8 soft
– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – Subroutine Library – Self Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – CP-2 Assembler – CP-2 Linkage Editor – CP-2 Program Validation Software – Subroutine Library – Self Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – Subroutine Library – Self Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – Subroutine Library – TC-2 Executive – TC-2 Program Validation – APL Programming Aids – S/360 and S/370 Source Maintenance Facility – Self Test
– Navigation/Threat Analysis (EA-6B)	– Navigation/Weapon Delivery (F-111)	– Navigation/Weapon Delivery (A-6)	– Navigation/Weapon Delivery (A-7D/E)
– Read-only storage; microprogram control	– Symmetrical interface on I/O channel allows multisystem usage – A third I/O channel can be added with minimal design changes – An auxiliary storage unit for expansion above 8K words is available	– Symmetrical interface on I/O channel allows multisystem usage – An auxiliary storage unit for expansion above 8K words is available	– Package and power figures given include a signal converter with 7 S/D and 8 DC/D input channels, and 6 D/S, 3 D/S (wheels), and 5 D/DC (including 2 spares) output channels. Also available without signal converter as TC-2 SSE. TC-2 SSE has additional 13-bit parallel I/O channel available externally.

Advanced System/4 Pi Computers

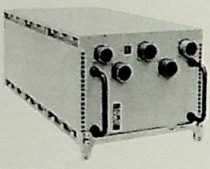
CP-1075/AYK

AP-1	AP-2	AP-101	CC-1
1506	1506	1508	54,400
36	36	44	870
7.6 x 12.7 x 15.6	7.6 x 12.7 x 15.6	7.62 x 10.12 x 19.56	68 x 40 x 20
200	200	340 with power switching[3] 370 without power switching[3]	4230
8K 8K/24K	8K 8K/24K	16K 8K/32K within structure, up to 256K with external memory units	128K 64K/176K
32	32	32	32
0.45 1.0	0.45 1.0	0.45 0.9	0.45 1.0
Monolithic[2]	Monolithic[2]	Monolithic[2]	Monolithic[2]
450 2.0 6.8 10.8 83 No Four 16-bit serial MPX, 8 DO, 4 DI, and 16 interrupts with 9 priority levels	430 2.0 6.8 10.8 83 No Two 16-bit serial MPX, 4 DI, 5 DO, and 12 interrupts with 7 priority levels	500 1.65[4] 5.2[4] 9.0[4] 151 Yes One 17-bit (16 data, 1 parity) parallel multiplexer channel, DMA, and buffered and direct I/O with up to 450,000 halfwords per second	740 0.5 - 0.9 3.4 8.3 166 Yes Two multiplex channels, one channel has 8 high-speed subchannels and the other has 56 medium-speed subchannels
Eight general-purpose	Eight general-purpose	– Eight fixed-point general-purpose hardware (2sets) – Eight floating point hardware registers	16 general-purpose (4 sets)
– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – Subroutine Library – Self Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – Subroutine Library – Onboard Program Validation – Self Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – AP-101 Program Validation Software – Functional Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – S/360 and S/370 JOVIAL Compiler – CC-1 JOVIAL Compiler – CC-1 Operating System – Subroutine Library – Self Test – Maintenance Software (In-flight performance, premission readiness, and diagnostic maintenance programs)
– Navigation/Weapon Delivery and Data Management (F-15)	– Central Integrated Test System	– Data Management – Guidance – Navigation/Weapon Delivery	– Command and Control – Signal Processing – Multiprocessing (AWACS)
– Storage efficiency using 16-bit or 32-bit data and instructions	– Storage efficiency using 16-bit or 32-bit data and instructions	– Storage efficient architecture,(16 bit and 32-bit data and instructions) – Halfword storage protect – Halfword parity – Read-only storage, micro-programmed control – Memory power switching option – Addressing to 512K halfwords – External main store interface option – Hexadecimal floating point – Multicomputer and Multiprocessor options – Optional custom micro-programmed instructions and functions – Problem/supervisor states – Comprehensive BITE	– Cache organization (Cache storage is monolithic) – S/370 compatible (planned option) – Read-only storage; micro program control – Optimized for maintainability

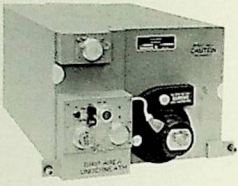
Advanced System/4 Pi Computers		
		CP-1125/BQQ-5
SP-0	SP-1	SP-201
16/page	560	15,970 (with growth available)
1.2/page	18.1	660
3.6 x 8.0 x 0.5/page	4.2 x 10.2 x 13.6	45.5 x 19.5 x 18.0
51	72	1095 at 60 Hz, 950 average, 865 at 400 Hz
4 K[5] 4K/16K	4K[6] 4K/16K	32K 16K/48K
16	16	16
0.6 1.5 (effective)	0.6 1.3	0.45 1.0
Monolithic[2]	Monolithic[2]	Monolithic[2]
230 3.5 11.0 24.0 33 No 16-bit parallel, basic channel has break-in and direct I/O modes	342.5 2.7 5.3 8.0 41 No 16-bit parallel, I/O modes: DMA, buffered and direct, customized I/O	450 1.67 6.67 7.33 43 No Two 32-bit DMA, MPX, 8 subchannels, break-in, multiple interrupts, 32-bit I/O channel
Two (A, B)	Three (A, B, Q)	Three (A, B, Q)
– S/360 and S/370 Assembler – S/360 and S/370 Functional Simulator – Subroutine Library – Self Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – SP-1 Assembler – SP-1 Linkage Editor – SP-1 Program Validation – Library Utilities – Self Test	– S/360 and S/370 Assembler – S/360 and S/370 Linkage Editor – S/360 and S/370 Functional Simulator – Performance Monitor/ Fault Location
– Medium Performance Subsystem Processor – S-3A Subsystem Control with monolithic memory (SP-0A) – Midcourse Guidance Unit (Harpoon Missile) with DRO core memory (SP-0B)	– High Performance Subsystem Processor – F-4 ATIS – Navigation, Missile and Drone Stabilization and Control, Communications Processor – Torpedo Stabilization and Control	System processing and controlling (AN/BQQ-5)
The SP-0 features a one page CPU. The SP-0A has a one page 4K monolithic memory and a one page special I/O. The SP-0B has a one page DRO core memory and a one page special I/O. A monolithic memory will be available for the SP-0B in mid-1974	The SP-1 structure has sufficient space for a 16K memory and customized I/O. Provisions for double-precision arithmetic are included. The SP-1A is essentially the same as an SP-1, but does not have a structure or power supply. It weighs 3.6 pounds and occupies 100 cubic inches. The SP-1B is for nonflight environments and uses dual-in-line packaging (DIP). It weights 200 pounds and occupies 8 cubic feet. The SP-1M extends the SP-1 performance by including Load Double, Store Double, and long-format Register-Storage (RS) instructions.	– Hybrid System/4 Pi and SHP packaging – Very maintainable – NTDS interface

Models of System/4 Pi and Advanced/4 Pi Computers

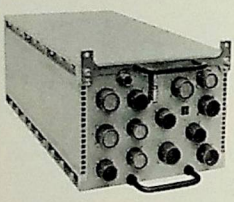
CP-1



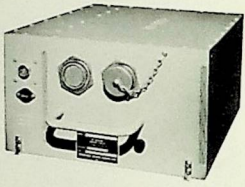
TC-2



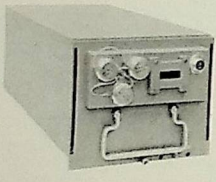
CP-1
Coupler



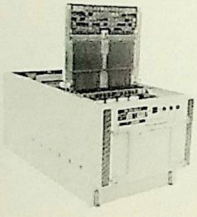
AP-1 or
AP-2



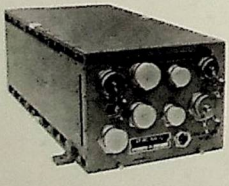
CP-2



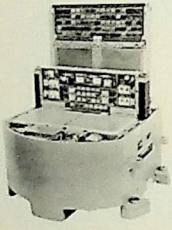
SP-0A



CP-3



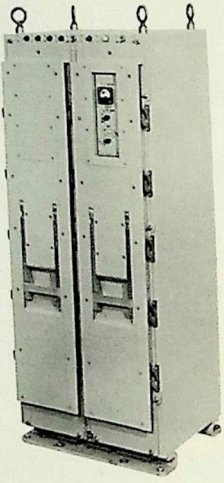
SP-0B



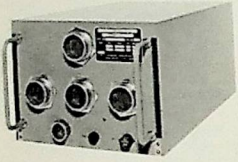
See Tables for Accurate Relationship

SP-1

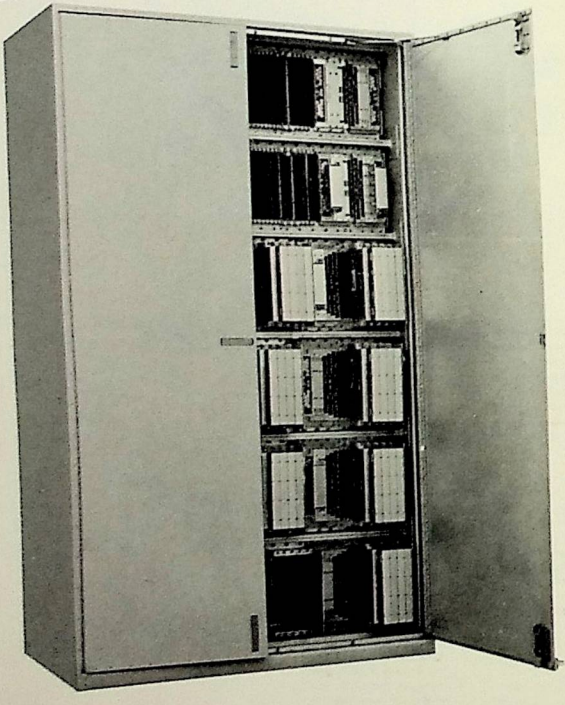
SP-201



AP-101



CC-1



LEGEND:

DC/D	Direct-current-to-digital convertor
D/DC	Digital-to-direct-current converter
DI	Discrete inputs
DMA	Direct memory access
DO	Discrete outputs
DRO	Destructive readout
D/S	Digital-to-synchro converter
ECI	Externally controlled input
ECO	Externally controlled output
IC	Integrated circuit (mostly small-scale-integration transistor transistor logic)
K	1024 (core-storage multiplier)
kop/s	Thousands of operations per second
MPX	Multiplex(er) (ing)
PCI	Program-controlled input
PCO	Program-controlled output
S/D	Synchro-to-digital converter
SHP	Standard Hardware Program (Navy)
S/360	Resembles and is compatible with IBM System/360 machines and software
S/370	Resembles and is compatible with IBM System/370 machines and software

NOTES:

[1] 16K configuration requires auxiliary memory unit.

[2] Unit logic and medium-scale integration transistor transistor logic.

[3] Values stated are for a 32K memory configuration and maximum performance.

[4] Calculated execution times.

[5] SP-0A has a monolithic memory, while the SP-0B uses a core memory. An SP-0B monolithic memory will be available in mid-1974.

[6] Alternate monolithic memory available in mid-1974.

System/4 Pi
Computers

IBM System/4 Pi is the family name for a series of general-purpose, military digital computers based on common technology.

The name 4 Pi derives from the geometrical 4π, which is the number of steradians making up a full sphere. System/4 Pi also fills a sphere - the full spectrum of military computer needs - for airborne, space, or shipboard use.

Introduced in 1966, this design concept includes sufficient growth potential to respond to a wide range of real-time data-handling requirements. Cost-effective as well, System/4 Pi computers have fully met the demands of several avionic systems in EA-6B, F-111, A-7D/E, A-6E, and S3-A aircraft, and are now being produced for the AN/BQQ-5 Sonar Set, Harpoon naval applications, and AWACS.

Three basic types of computers made up the original System/4 Pi line: the customized processor (CP) series, the tactical computer (TC), and the extended performance (EP) machines; a multiprocessor configuration of the EP was called the EP/MP. Some of these earlier computers are deleted from the detailed characteristics listing because they have been replaced by Advanced System/4 Pi computers.

Advances in MSI logic and the development of 1-μs storage led IBM to introduce the Advanced System/4 Pi series early in 1970. Advanced System/4 Pi computers now include three types, arranged according to architecture: the advanced processor (AP) series, the command and control (Model CC), and the subsystem processor (SP) machine.

For further information contact your IBM FSD Marketing Representative or

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System/4 Pi computers are manufactured by the IBM Federal Systems Division, Electronics Systems Center, Owego, New York, and are available only to the U.S. Government or its prime contractors or subcontractors.